

Abstract of the Disclosure

In a method of forming a self-aligned contact, gates are formed on a semiconductor substrate in a striped pattern. Bit lines are formed in a striped pattern that extends cross-wise to the gates. The bit lines are isolated from one another by a first interlayer insulation layer. Next, a second interlayer insulation layer is formed between the bit lines, and a photoresist film pattern is formed on the second interlayer insulation layer. The photoresist film pattern is used for forming contact holes extending between the gates down to conductive pads. The contact holes are filled to form conductive plugs that contact the conductive pads. The photoresist film pattern is formed as a series of stripes which extend parallel to the gates. The stripes of photoresist expose segments of the bit lines and the portions of the second interlayer insulation layer disposed directly above the conductive film pads, thereby securing a sufficient alignment margin, and exposing a large underlying area to be etched in forming the contact holes. To form a semiconductor device, a third interlayer insulation layer, an etch stop layer, an oxide layer and a hard mask layer are formed on the conductive plugs. Next, a second photoresist film pattern is formed on the hard mask layer. The hard mask layer and the oxide layer are etched using the second photoresist film pattern as an etching mask until the etch stop layer is exposed. Second contact holes for use in forming capacitor lower electrodes are formed by sequentially removing the exposed etching stop layer and the exposed third interlayer insulation layer using the hard mask layer as an etching mask, until the second contact holes expose the conductive plugs.